

What is claimed is:

1 1. A buffer layer, suitable for a substrate of a
2 thin film transistor (TFT), comprising:

3 an amorphous layer, deposited on the substrate; and

4 an oxide-containing layer, deposited on the
5 amorphous silicon layer.

1 2. The buffer layer as claimed in claim 1, wherein
2 the oxide-containing layer comprises silicon oxide (SiO_x).

1 3. The buffer layer as claimed in claim 1, wherein
2 the oxide-containing layer is a crystallized layer.

3 4. The buffer layer as claimed in claim 1, wherein
4 the thickness of the oxide-containing layer is about
5 1000~2000Å.

1 5. The buffer layer as claimed in claim 1, wherein
2 the oxide-containing layer is formed by plasma enhanced
3 chemical vapor deposition (PECVD).

1 6. The buffer layer as claimed in claim 1, wherein
2 the density of the oxide-containing layer is about
3 2.0~2.2 g/cm³.

1 7. The buffer layer as claimed in claim 1, wherein
2 the amorphous layer comprises amorphous silicon.

3 8. The buffer layer as claimed in claim 1, wherein
4 the thickness of the amorphous layer is about 250~1000Å.

1 9. The buffer layer as claimed in claim 1, wherein
2 the density of the amorphous layer is about 2.0~2.3 g/cm³.

1 10. The buffer layer as claimed in claim 1, wherein
2 the hydrogen content of the amorphous layer is about
3 5~10%.

1 11. The buffer layer as claimed in claim 1, wherein
2 the amorphous layer is formed by plasma enhanced chemical
3 vapor deposition (PECVD).

1 12. The buffer layer as claimed in claim 1, wherein
2 the buffer layer further comprises a nitride layer
3 deposited between the substrate and the amorphous layer.

1 13. The buffer layer as claimed in claim 12,
2 wherein the nitride layer comprises silicon nitride.

1 14. The buffer layer as claimed in claim 1, wherein
2 the hydrogen content of the amorphous layer is less than
3 10%.

1 15. A thin film transistor having a buffer layer
2 for promoting electron mobility, comprising:

3 a substrate;

4 a buffer layer, comprising:

5 an amorphous layer, deposited on the substrate; and

6 a crystallized layer, deposited on the amorphous
7 layer;

8 an active layer, deposited on the crystallized
9 layer;

10 an insulating layer, covered conformally on the
11 active layer, the amorphous layer, crystallized
12 layer and the side walls of the active layer;

13 a conductive layer, deposited on the insulating
14 layer above parts of the active layer; and
15 a dielectric layer, completely covering the
16 crystallized layer and the conductive layer.

1 16. The buffer layer as claimed in claim 15,
2 wherein the crystallized layer comprises oxide.

1 17. The buffer layer as claimed in claim 15,
2 wherein the thickness of the crystallized layer is about
3 1000~2000Å.

1 18. The buffer layer as claimed in claim 15,
2 wherein the amorphous layer comprises amorphous silicon.

1 19. The buffer layer as claimed in claim 15,
2 wherein the thickness of the amorphous layer is about
3 1000~2000Å.

1 20. The buffer layer as claimed in claim 15,
2 wherein the hydrogen content of the amorphous layer is
3 less than 10%.

1 21. The buffer layer as claimed in claim 15,
2 wherein the buffer layer further comprises silicon
3 nitride deposited between the substrate and the amorphous
4 layer.